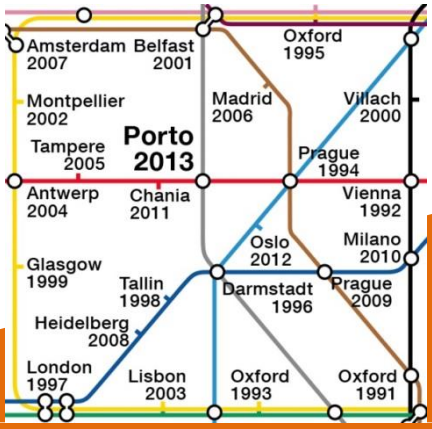
23RD INTERNATIONAL CONFERENCE ON FIELD PROGRAMMABLE LOGIC AND APPLICATIONS

PORTO, PORTUGAL
SEPT. 2-4, 2013



23RD INTERNATIONAL CONFERENCE ON FIELD PROGRAMMABLE LOGIC AND APPLICATIONS (FPL 2013)

Conference Guide

www.fpl2013.org

Notes:

Welcome Message

The 23rd International Conference on Field Programmable Logic and Applications (FPL 2013) aims to bring together researchers and practitioners of reconfigurable and field-programmable technologies from both academia and industry.

This year's FPL conference offers a very diverse technical program and exciting social events. The technical program is organized as 18 concurrent technical sessions for which we had 273 original submissions (233 regular papers, 18 PhD Forum papers, and 22 Demo Night proposals). Of the 233 regular paper submissions, the technical program committee selected 53 for oral presentation as regular/full papers (acceptance rate of 23%) and 73 for poster presentation as short papers. Ten of the 18 PhD Forum submissions were accepted and 17 of the 22 Demo Night proposals were selected for presentation. This large number of Demo submissions reveals not only a great interest in this year's FPL event, but most importantly a high-level of maturity of tools developed in academia that researchers are increasingly willing to share with the community at large. As with previous FPL programs, this year's program includes five Workshops from both academia and industry and one Tutorial in addition to four poster sessions and one PhD Forum poster session. Lastly, the program includes a special panel session on EU Horizon 2020 Reconfigurable Computing Funding Opportunities and four high-profile keynote presentations featuring leading industrial participants from Xilinx Inc., Altera Corp., Google Inc. and Microsoft Corp.

We note the participation of various industrial partners from the more traditional reconfigurable computing domains to newer FPGA-based applications domains, including: Altera Corp, Xilinx, Inc., Microsemi Corp, The Dini Group, Sigasi nv, and Solarflare Comm., Inc. Interest from this variety of industrial sources is clear evidence that reconfigurable technology is maturing and permeating the computing market.

We wish to thank all members of the organization, steering and program committees, all reviewers, all sponsors, all keynote speakers, and all authors of papers submitted to FPL. They all contributed to an interesting and inspiring program.

We thank you for joining us at Porto, Portugal, and enjoy the exciting technical and social program at this year's FPL 2013.

João M.P. Cardoso
Universidade do Porto, Porto, Portugal (jmpc@acm.org)
(FPL 2013 General Chair)

Pedro C. Diniz
USC Information Sciences Institute, USA (pedro@isi.edu)
(FPL 2013 Program Co-Chair)

Katherine (Compton) Morrow
University of Wisconsin-Madison, Madison, USA (kati@engr.wisc.edu)
(FPL 2013 Program Co-Chair)

Table of Contents

Schedule

Sunday, September 1st

		Ipanema Park Hotel		
		Sunday, Sept. 1		
		Bar Twin Towers	Room Ipanema	Room Porto
8:15	-		Registration	
9:00	10:45		Altera Workshop	HPCW'13
10:45	11:30		Coffee-Break + Poster Sessions	
11:30	12:30		Altera Workshop	HPCW'13
12:30	14:00		Lunch	
14:00	15:30		Altera Workshop	HPCW'13
15:30	16:15		Coffee-Break + Poster Sessions	
16:15	18:00		Altera Workshop	HPCW'13
18:30	20:30	Cocktail Reception Hosted by Solarflare Comm., Inc.		

HPCW'13: Workshop on Research Projects Focusing on High Perform

Monday-Tuesday, September 2nd-3rd

		Ipanema Park Hotel		
		Monday, Sept. 2		
		Room Ipanema	**Room Porto**	**Room Granja**
8:00	-	**Registration**		
8:40	**9:00**	Welcome Session		
9:00	**10:00**	**Keynote (room Ipanema)** **Gordon Brebner, Xilinx Labs, Ireland**		
10:00	**10:30**	**PhD-Elevator Pitch**		
10:30	**11:10**	Coffee-Break + Poster Session PS1 (PhD Forum)		
11:10	**12:30**	M1A	M1B	M1C
12:30	**14:00**	Lunch		
14:00	**15:20**	M2A	M2B	M2C
15:20	**16:05**	Coffee-Break + Poster Session PS2		
16:05	**17:25**	M3A	M3B	M3C
17:25	**19:00**	Break		
19:00	**21:30**	**Demo Night + hors d'oeuvres**		

BOF: Birds-of-a-Feather

		Ipanema Park Hotel		
		Tuesday, Sept. 3		
		Room Ipanema	**Room Porto**	**Room Granja**
8:15	-	**Registration**		
8:30	**9:00**	Announcements		
9:00	**10:00**	**Keynote (room Ipanema)** **Sean Atsatt, Altera Corp., USA**		
10:00	**10:55**	Coffee-Break + Poster Session PS3		
10:55	**12:15**	T1A	T1B	T1C
12:30	**14:00**	Lunch		
14:00	**14:55**	T2A	T2B	T2C
14:55	**15:40**	Coffee-Break + Poster Session PS4		
15:40	**17:40**	Industry Sess.	BOF #1 Sess.	BOF #2 Sess.
18:00	**18:30**	Departure to Taylor's Port Wine Cellars		
18:30	**19:30**	**Visit to Taylor's Port Wine Cellars**		
19:30	**23:00**	**Banquet at Barão Fladgate (Taylor's Restaurant)**		
23:00	**23:20**	Return to Hotel		

Wednesday, September 4th

		Ipanema Park Hotel		
		Wednesday, Sept. 4		
		Room Ipanema	**Room Porto**	**Room Granja**
8:15	-	**Registration**		
8:30	**8:50**	Announcements (**room Ipanema**)		
8:50	**9:50**	**Keynote** (**room Ipanema**) **Satnam Singh, Google Inc., USA**		
9:50	**10:35**	Coffee-Break + Poster Session PS5		
10:35	**12:20**	W1A	W1B	W1C
12:30	**14:00**	Lunch		
14:00	**15:00**	**Keynote** (**room Ipanema**) **Ken Eguro, Microsoft Research in Redmond, Washington, USA**		
15:00	**15:15**	Closing Remarks (**room Ipanema**)		
15:15	**15:45**	Coffee-Break		
15:45	**17:15**	Presentations and Panel: EU Horizon 2020 Reconfigurable Computing Funding Opportunities		
17:15	**17:30**	Closing Session (**room Ipanema**)		
17:30	**20:00**	**Ribeira Trip**		

Thursday-Friday, September 5th-6th

		FEUP				FEUP	
		Thursday, Sept. 5				**Friday, Sept. 6**	
		Room I221	Room B008	Room B009		**Room I221**	Room B008
8:30	-	**Registration**			8:30	-	**Registration**
9:00	**10:45**	Xilinx Workshop	SRCS'13	ERA	9:00	**10:45**	Xilinx Workshop	CER'13
10:45	**11:30**	Coffee-Break + Poster Sessions (**room I-105**)			10:45	**11:30**	Coffee-Break + Poster Sessions (**room I-105**)	
11:30	**12:30**	Xilinx Workshop	SRCS'13	ERA	11:30	**12:30**	Xilinx Workshop	CER'13
12:30	**14:00**	Lunch			12:30	**14:00**	Lunch	
14:00	**15:30**	Xilinx Workshop	SRCS'13		14:00	**15:30**	Xilinx Workshop	CER'13
15:30	**16:15**	Coffee-Break + Poster Sessions (**room I-105**)			15:30	**16:15**	Coffee-Break + Poster Sessions (**room I-105**)	
16:15	**18:00**	Xilinx Workshop	SRCS'13		16:15	**18:00**	Xilinx Workshop	CER'13

SRCS'13: 2nd Workshop on Self-Awareness in Reconfigurable Computing Systems
CER'13: Challenges of Embedded Robotics: Can FPGAs Overcome Them?
ERA: Embedded Reconfigurable Architectures

Overall Program

Sunday, Sept. 1

17:30 - 20:00	**Registration**
18:30 - 20:30	**Cocktail Reception (hosted by Solarflare Comm., Inc.)**

Monday, Sept. 2

08:00 - 08:40	**Registration**
08:40 - 09:00	**Welcome Session**
09:00 - 10:00	**Keynote #1:** **Programmable Logic in a Software Person's World** *Gordon Brebner, Xilinx Labs, Ireland* Chair: Pedro C. Diniz (USC Information Sciences Institute, USA)
10:00 - 10:30	**PhD Forum Elevator Pitch** Chair: Stephan Wong, TU Delft, The Netherlands
10:30 - 11:10	**Coffee Break and Poster Session #1 (PhD Forum)**
11:10 - 12:30	**Session M1A: Infrastructure, Interconnect and Communication** Session Chair: Peter Cheung (Imperial College London, UK) **Automated Synthesis of FPGA-Based Heterogeneous Interconnect Topologies** *Alessandro Cilardo, Edoardo Fusella, Luca Gallo, Antonino Mazzeo* **Generating Infrastructure for FPGA-Accelerated Applications** *Myron King, Asif Khan, Abhinav Agarwal, Oriol Arcas, Arvind* **The Power of Communication: Energy-Efficient NoCs for FPGAs** *Mohamed Abdelfattah, Vaughn Betz*
	Session M1B: Defects, Faults, and Aging Session Chair: Kentaro Sano (Tohoku University, Japan) **Altering LUT Configuration for Wear-Out Mitigation of FPGA-Mapped Designs** *Parthasarathy Murali Baskar Rao, Abdulazim Amouri, Saman Kiamehr, Mehdi Tahoori* **Improving Autonomous Soft-Error Tolerance of FPGA Through LUT Configuration Bit Manipulation** *Anup Das, Shyamsundar Venkataraman, Akash Kumar* **Defect-Robust FPGA Architectures for Intellectual Property Cores in System LSI** *Motoki Amagasaki, Kazuki Inoue, Qian Zhao, Masahiro Iida, Morihiro Kuga, Toshinori Sueyoshi*

	Session M1C: Application Acceleration
	Session Chair: Oliver Diesel (University of New South Wales, Australia)
	Accelerating Random Forest Training Process Using FPGA *Chuan Cheng, Christos- Savvas Bouganis*
	FPGA-Based K-Means Clustering Using Tree-Based Data Structures *Felix Winterstein, Samuel Bayliss, George A. Constantinides*
	Accelerating Maximum Likelihood Estimation for Hawkes Point Processes *Ce Guo, Wayne Luk*
12:30 - 14:00	**Lunch**
14:00 - 15:20	**Session M2A: FPGA Infrastructure and Design Environments**
	Session Chair: Diana Göhringer (Ruhr-Universität Bochum, Germany)
	Titan: Enabling Large and Complex Benchmarks in Academic CAD *Kevin E. Murray, Scott Whitty, Suya Liu, Jason Luu, Vaughn Betz*
	RIFFA 2.0: A Reusable Integration Framework for FPGA Accelerators *Matthew Jacobsen, Ryan Kastner*
	In Pursuit of Instant Gratification for FPGA Design *Andrew Love, Wenwei Zha, Peter Athanas*
	Session M2B: Application Acceleration
	Session Chair: Olivier Sentieys (INRIA, University of Rennes, France)
	A Fully Pipelined FPGA Architecture for Stochastic Simulation of Chemical Systems *David B. Thomas, Hideharu Amano*
	A Hardware Accelerated Approach for Imaging Flow Cytometry *Dajung Lee, Pingfan Meng, Matthew Jacobsen, Henry Tse, Dino Di Carlo, Ryan Kastner*
	Accelerating Solvers for Global Atmospheric Equations Through Mixed-Precision Data *Flow Engine* *Lin Gan, Haohuan Fu, Wayne Luk, Chao Yang, Wei Xue, Xiaomeng Huang, Youhui Zhang, Guangwen Yang*
	Session M2C: FPGA Architecture
	Session Chair: Leonel Sousa (Instituto Superior Técnico / INESC-ID, Portugal)
	Charge Recycling for Power Reduction in FPGA Interconnect *Safeen Huda, Jason Anderson, Hirotaka Tamura*
	Impact of Hard Macro Size on FPGA Clock Rate and Place/Route Time *Chris Lavin, Brent Nelson, Brad Hutchings*
	Should FPGAs Abandon the Pass-Gate? *Charles Chiasson, Vaughn Betz*
15:20 - 16:05	**Coffee Break and Poster Session #2**

16:05 - 17:25	**Session M3A: Placement and Routing** Session Chair: Tobias Becker (Imperial College London, UK) **StaticRoute: A Novel Router for the Dynamic Partial Reconfiguration of FPGAs** *Brahim Al Farisi, Karel Bruneel, Dirk Stroobandt* **Criticality-Based Routing for FPGAs with Reverse Body Bias Switch Box Architectures** *Wei Ting Loke, Wenfeng Zhao, Yajun Ha* **A Run-Time Graph-Based Polynomial Placement and Routing Algorithm for Virtual FPGAs** *Ricardo Ferreira, Luciana Rocha, Andre G. dos Santos, Jose A. Nacif, Stephan Wong, Luigi Carro*
	Session M3B: Architecture Session Chair: Horácio C. Neto (IST/INESC-ID, Portugal) **A High-Performance Overlay Architecture for Pipelined Execution of Data Flow Graphs** *Davor Capalija, Tarek Abdelrahman* **Efficient Implementation of Virtual Coarse Grained Reconfigurable Arrays on FPGAs** *Karel Heyse, Tom Davidson, Elias Vansteenkiste, Karel Bruneel, Dirk Stroobandt* **An Efficient FPGA Overlay for Portable Custom Instruction Set Extensions** *Dirk Koch, Christian Beckhoff, Guy G.F. Lemieux*
	Session M3C: Networking Applications Session Chair: Teresa Riesgo (Universidade Politécnica de Madrid, Spain) **A Packet Classifier Using LUT Cascades Based on EVMDDs(k)** *Hiroki Nakahara, Tsutomu Sasao, Munehiro Matsuura* **Memory Efficient IP Lookup in 100 Gbps Networks** *Jiří Matoušek, Martin Skačan, Jan Kořenek* **A Flexible Hash Table Design for 10GBPs Key-Value Stores in FPGAs** *Zsolt István, Gustavo Alonso, Michaela Blott, Kees Vissers*
17:25 - 19:00	**Break**
19:00 - 21:30	**Demo Night (including hors d'oeuvres and drinks)** Demo Night Chair: José G. F. Coutinho (Imperial College London, UK)

Tuesday, Sept. 3

08:00 - 08:40	**Registration**
08:30 -09:00	**Announcements**
09:00 - 10:00	**Keynote #2** **Architecting SOC FPGA's** *Sean Atsatt, Altera Corp., USA* Chair: Katherine (Compton) Morrow (University of Wisconsin-Madison, USA)

10:00 - 10:55	**Coffee Break and Poster Session #3**
10:55 - 12:15	**Session T1A: Run-Time Reconfiguration** Session Chair: João Canas Ferreira (FEUP, Universidade do Porto, Portugal) **Weighted Partitioning of Sequential Processing Chains for Dynamically Reconfigurable FPGAs** *Michael Feilen, Andreas Iliopoulos, Michael Vonbun, Walter Stechele* **Optimizing Under Abstraction: Using Prefetching to Improve FPGA Performance** *Hsin-Jung Yang, Kermin Fleming, Michael Adler, Joel Emer* **Run-Time Optimization of a Dynamically Reconfigurable Embedded System Through Performance Prediction** *Giovanni Mariani, Vlad-Mihai Sima, Gianluca Palermo, Vittorio Zaccaria, Giacomo Marchiori, Cristina Silvano, Koen Bertels*
	Session T1B: Security Applications Session Chair: Guy Gogniat (University Bretagne-Sud, France) **A Secure Coprocessor for Database Applications** *Arvind Arasu, Ken Eguro, Raghav Kaushik, Donald Kossmann, Ravi Ramamurthy, Ramaratnam Venkatesan* **Fast, FPGA-Based Rainbow Table Creation for Attacking Encrypted Mobile Communications** *Panos Papantonakis, Charalampos Manifavas, Dionisios Pnevmatikatos, Ioannis Papaefstathiou* **FPGA Based ReKeying for Cryptographic Key Management in Storage Area Network** *Yi Wang, Yajun Ha*
	Session T1C: Biosensing and Imaging Applications Session Chair: Peter Athanas (Virginia Polytechnic Institute, USA) **An FPGA Design for High Speed Feature Extraction from a Compressed Measurement Stream** *Dustin Richmond, Ryan Kastner, Ali Irturk, John McGarry* **FPGA Implementation of Hierarchical Enumerative Coding for Locally Stationary Image Source** *Yuhui Bai, Syed Zahid Ahmed, Bertrand Granado* **Scalable and High Throughput Biosensing Platform** *José Leitão, José Germano, Nuno Roma, Ricardo Chaves, Pedro Tomás*
12:30 - 14:00	**Lunch**
14:00 - 14:55	**Session T2A: Floating-Point Arithmetic** Session Chair: Dirk Stroobandt (University of Ghent, Belgium) **Efficient Floating-Point Polynomial Evaluation on FPGAs** *Martin Langhammer, Bogdan Pasca* **Iterative Floating Point Computation Using FPGA DSP Blocks** *Fredrik Brosser, Hui Yan Cheah, Suhaib Fahmy*

	Session T2B: Fault-Tolerance and Scrubbing Session Chair: Minoru Watanabe (Shizuoka University, Japan) **Radiation Mitigation Efficiency of Scrubbing on the FPGA Based CBM-ToF Read-Out Controller** *Sebastian Manz, Jano Gebelein, Andrei Oancea, Heiko Engel, Udo Kebschull* **Accelerated FPGA Repair through Shifted Scrubbing** *Gabriel Nazar, Leonardo P. Santos, Luigi Carro*
	Session T2C: Pattern Matching Applications Session Chair: Viktor Prasanna (University Southern California, USA) **Hardware-Accelerated Regular Expression Matching for High-Throughput Text Analytics** *Kubilay Atasu, Raphael Polig, Christoph Hagleitner, Frederick. R. Reiss* **Token-Based Dictionary Pattern Matching for Text Analytics** *Raphael Polig, Kubilay Atasu, Christoph Hagleitner*
14:55 - 15:40	**Coffee Break and Poster Session #4**
15:40 - 17:40	**Industry Session (Room Ipanema)** **Presentations from Industry** Chair: Sinan Kaptanoglu (Microsemi Corp., USA)
15:40 - 17:40	**BOF #1 - Birds-of-a-Feather (Room Porto)** **Just-in-Time Compilation and Runtime Implementation Techniques for FPGAs** Chairs: Christian Plessl (University of Paderborn, Germany), and Michael Hübner (Ruhr-Universität Bochum, Germany)
	BOF #2 - Birds-of-a-Feather (Room Granja) **High-Level Synthesis** Chairs: Kyle Rupnow (Nanyang Technological University, Singapore), and Nikolaos Kavvadias (Ajax Compilers, Athens, Greece)
18:00 - 18:30	**Hotel departure to Taylors Port Wine Cellars**
18:30 - 19:30	**Visit to Taylors Port Wine Cellars**
19:30 - 23:00	**Banquet at the Barão Fladgate Restaurant**
23:00 - 23:20	**Return to the Conference Hotel**

Wednesday, Sept. 4

08:00 - 08:40	**Registration**
08:30 - 08:50	**Announcements**
08:50 - 09:50	**Keynote #3** **Accelerating The Datacenter** *Satnam Singh, Google Inc., USA* Chair: Katherine (Compton) Morrow (University of Wisconsin-Madison, USA)
09:50 - 10:35	**Coffee Break and Poster Session #5**

10:35 - 12:20	**Session W1A: Soft Processor Systems and Memory**
	Session Chair: Markus Weinhardt (Osnabrück Hochschule, Germany)
	Low-Cost, High-Performance Branch Predictors for Soft Processors *Di Wu, Kaveh Aasaraai, Andreas Moshovos*
	TputCache: High-Frequency, Multi-Way Cache for High-Throughput FPGA Applications *Aaron Severance, Guy Lemieux*
	Managing the FPGA Memory Wall: Custom Computing or Vector Processing? *Matthew Naylor, Paul J. Fox, A. Theodore Markettos, Simon W. Moore*
	Session W1B: High-Level Synthesis and CAD
	Session Chair: David Andrews (University of Arkansas, USA)
	Rapid FPGA Design Prototyping Through Preservation of System Logic: A Case Study *Travis Haroldsen, Brent Nelson, Brad White*
	Dynamic Branch Prediction for High-Level Synthesis *Vianney Lapotre, Philippe Coussy, Cyrille Chavet, Hugues Wouafo, Robin Danilo*
	High-Level Synthesis with Behavioral Level Multi-Cycle Path Analysis *Hongbin Zheng, Swathi Gurumani, Liwei Yang, Deming Chen, Kyle Rupnow*
	Simulation-Based HW/SW Co-Debugging for Field-Programmable Systems-On-Chip *Ruediger Willenberg, Paul Chow*
	Session W1C: Arithmetic and Computation Cores
	Session Chair: Tim Todman (Imperial College London, UK)
	Multiple Constant Multiplication with Ternary Adders *Martin Kumm, Martin Hardieck, Jens Willkomm, Peter Zipf, Uwe Meyer-Baese*
	Arithmetic Core Generation Using Bit Heaps *Nicolas Brunie, Florent de Dinechin, Kinga Illyes, Matei Istoan, Bogdan Popa*
	Energy Efficient Parameterized FFT Architecture *Ren Chen, Hoang Le, Viktor K. Prasanna*
	Area/Performance Evaluation of Digit-Digit GF(2^k) Multipliers on FPGAs *Miguel Morales-Sandoval, Arturo Díaz-Pérez*
12:30 - 14:00	**Lunch**
14:00 - 15:00	**Keynote #4:**
	Reconfigurable Hardware at the World's Largest Software Company *Ken Eguro, Microsoft Research in Redmond, WA, USA* Chair: Ryan Kastner (UC San Diego, USA)
15:00 - 15:15	**Closing Remarks**
15:15 - 15:45	**Coffee Break**

15:45 - 17:15	**Presentations and Panel: EU Horizon 2020 Reconfigurable Computing Funding Opportunities** Moderator: Cristina Silvano (Politecnico di Milano, Italy) Invited Speakers: Panos Tsarchopoulos, Future and Emerging Technologies, EU Project Officer**;** Georgi Kuzmanov, ARTEMIS Joint Undertaking, Programme Officer
17:15 - 17:30	**Closing Session**
17:30 - 20:00	**Ribeira Trip**

Poster Presentations

Poster Session #1 (PhD Forum Papers)

Session Chair: Stephan Wong (TU Delft, The Netherlands)

Design Space Exploration based on MultiObjective Genetic Algorithms and Clustering-based High-Level Estimation
Luiz Martins and Eduardo Marques

A Dataflow-Inspired CGRA for Streaming Applications
Anja Niedermeier, Jan Kuper and Gerard J.M. Smit

FPGA Based Control for Real Time Systems
Shane Fleming and David Thomas

Pipelining Computing Stages in Configurable Multicore Architectures
Ali Azarian

Integration of a Multi-FPGA System in a Common Cluster Environment
Oliver Knodel and Rainer Spallek

A Space/Time Tradeoff Methodology Using Higher-Order Functions
Rinse Wester and Jan Kuper

Degradation in FPGAs: Monitoring, Modeling and Mitigation
Abdulazim Amouri and Mehdi Tahoori

Identifying Sequences of Optimizations for HW/SW Compilation
Ricardo Nobre

A Reconfigurable Computing Architecture Using Magnetic Tunneling Junction Memories
Victor Silva, Jorge Fernandes, Mário Véstias and Horácio Neto

Distributed Embedded Systems Design Using Petri Nets
Filipe Moutinho and Luis Gomes

Poster Session #2

Session Chair: Eduardo Marques (ICMC, Universidade de São Paulo, Brazil)

A Directional Coarse-Grained Power Gated FPGA Switch Box and Power Gating Aware Routing Algorithm
Chin Hau Hoo, Yajun Ha and Akash Kumar

Dependable Dynamic Partial Reconfiguration with Minimal Area & Time Overheads on Xilinx FPGAs
Stefano Di Carlo, Giulio Gambardella, Marco Indaco, Paolo Prinetto, Daniele Rolfo and Pascal Trotta

Bambu: A Modular Framework for the High Level Synthesis of Memory-Intensive Applications
Christian Pilato and Fabrizio Ferrandi

A Scalable Design Approach for Stencil Computation on Reconfigurable Clusters
Xinyu Niu, Jose G. F. Coutinho and Wayne Luk

Comparing and Combining GPU and FPGA Accelerators in an Image Processing Context
Bruno da Silva, An Braeken, Erik H. D'Hollander, Abdellah Touhafi, Jan G. Cornelis and Jan Lemeire

TILT: A Multithreaded VLIW Soft Processor Family
Kalin Ovtcharov, Ilian Tili and J. Gregory Steffan

FPGA Based Hardware-Software Co-Designed Dynamic Binary Translation System
Yuan Yao, Zhongyong Lu, Qingsong Shi and Wenzhi Chen

FPGA IP Protection by Binding Finite State Machine to Physical Unclonable Function
Jiliang Zhang, Yaping Lin, Yongqiang Lyu, Gang Qu, Ray C.C. Cheung, Wenjie Che, Qiang Zhou and Jinian Bian

A Hardware Security Scheme for RRAM-based FPGA
Yi-Chung Chen, Wei Zhang and Hai Li

Accurate and Flexible Flow-Based Monitoring for High-Speed Networks
Marco Forconesi, Gustavo Sutter, Sergio Lopez-Buedo and Javier Aracil

A High-Performance IPV6 Lookup Engine on FPGA
Thilan Ganegedara and Viktor Prasanna

High Performance Architecture for Object Detection in Streamed Videos
Pavel Zemcik, Roman Juranek, Petr Musil, Martin Musil and Michal Hradis

FPGA-Accelerated Sliding Window Classifier with Structured Features
Ondrej Sychrovsky, Martin Matousek and Radim Sara

Performance Evaluation of Sparse Matrix-Matrix Multiplication
Shweta Jain-Mendon and Ron Sass

Aging-Based Leakage Energy Reduction in FPGAs
Sheng Wei, Jason Zheng and Miodrag Potkonjak

Poster Session #3

Session Chair: João Bispo (FEUP, Universidade do Porto, Portugal)

A Novel Net-Partition-Based Multithread FPGA Routing Method
Chun Zhu, Jian Wang and Jinmei Lai

A Platform-Independent Runtime Methodology for Mapping Multiple Applications onto FPGAs Through Resource Virtualization
Harry Sidiropoulos, Peter Figuli, Kostas Siozios, Dimitrios Soudris and Jürgen Becker

Timing-Constrained Minimum Area/Power FPGA Memory Mapping
Fangqing Du, Colin Yu Lin, Xiuhai Cui, Feng Liu, Fei Liu and Haigang Yang

Shadow And-Inverter Cones
Hadi Parandeh-Afshar, Grace Zgheib, David Novo, Madhura Purnaprajna and Paolo Ienne

Analyzing the Thermal Hotspots in FPGA-Based Embedded Systems
Hussam Amrouch, Thomas Ebi, Josef Schneider, Sridevan Parameswaran and Jörg Henkel

Energy Efficient Architecture for Matrix Multiplication on FPGAs
Kiran Matam, Hoang Le and Viktor Prasanna

An Asynchronous Bus Bridge for Partitioned Multi-SoC Architectures on FPGAs
Daniel Kliem and Sven-Ole Voigt

An Open-Source Multi-FPGA Modular System for Fair Benchmarking of True Random Number Generators
Viktor Fischer, Patrick Haddad and Florent Bernard

Towards Bounded Error Recovery Time in FPGA-based TMR Circuits using Dynamic Partial Reconfiguration
Ediz Cetin, Oliver Diessel, Lingkan Gong and Victor Lai

Compact Implementation of CCM and GCM modes of AES using DSP blocks
Antonio de la Piedra, Abdellah Touhafi and An Braeken

Design of a Multi GBPS Single Carrier Digital Baseband for 60GHz Applications and its FPGA Implementation
Surendra Guntur, Feike Jansen, Jan Hoogerbrugge, Lotfi Abkari and Eric Vos

A Single-Precision Compressive Sensing Signal Reconstruction Engine on FPGAs
Fengbo Ren, Richard Dorrance, Wenyao Xu and Dejan Marković

A Study of a Three-Dimensional Multiphase-Flow Simulator
Kenta Fujinami, Yoshiki Yamaguchi, Akira Sugiura and Yuetsu Kodama

Weasel: A Platform-Independent Streaming-optimized SATA Controller
Patrick Lehmann, Thomas Frank, Oliver Knodel, Steffen Köhler, Thomas B. Preußer and Rainer G. Spallek

Poster Session #4

Session Chair: Nuno Roma (Instituto Superior Técnico /INESC-ID, Portugal)

A Variation-Adaptive Retiming Method Exploiting Reconfigurability
Zhenyu Guan, Justin S. J. Wong, Sumanta Chaudhuri, George Constantinides and Peter Y. K. Cheung

An Event-Based Middleware for the Remote Management of Runtime Hardware Reconfiguration
François Philipp and Manfred Glesner

Timing Driven RTL-to-RTL Partitioner for Multi-FPGA Systems
Tobias Strauch

Shared Memory Heterogeneous Computation on PCIe-supported Platforms
Sambit Shukla, Yang Yang, Laxmi Bhuyan and Philip Brisk

A Resource-Efficient Probabilistic Fault Simulator
David May and Walter Stechele

Generation of Application Specific Heterogeneous Multi-Core Systems from Multithreaded Software
Alexander Wold, Jim Tørresen and Andreas Agne

Design Space Explorations of Hybrid-Partitioned TCAM (HP-TCAM)
Zahid Ullah, Manish Kumar Jaiswal and Ray C.C. Cheung

On Measurement of Parameters of Programmable Microelectronic Nanostructures Under Accelerating Extreme Conditions
Petr Pfeifer and Zdenek Pliva

Hardware-efficient Implementation of a Femtocell/Macrocell Interference-Mitigation Technique for High-performance LTE-Based Systems
Oriol Font-Bach, Nikolaos Bartzoudis, Miquel Payaró and Antonio Pascual-Iserte

A CMOS FIELD Programmable Analog Array for Intelligent Sensory Application
Cheng Xiaoyan, Yin Tao, Wu Qisong and Yang Haigang

A Low-Complexity Implementation of QC-LDPC Encoder in Reconfigurable Logic
Georgios Tzimpragos, Christoforos Kachris, Dimitrios Sourdris and Ioannis Tomkos

Fast Dynamically Updatable Packet Classifier on FPGA
Yun Qu and Viktor Prasanna

A Digital Architecture for Real-time Nonuniformity Correction of Infrared Focal-Plane Arrays
Rodolfo Redlich and Miguel Figueroa

Binarization Based Implementation for Real-time Human Detection
Shuai Xie, Yibin Li, Zhiping Jia and Lei Ju

Magnitude Modulation on Reconfigurable Computing Devices
Marco Gomes, Vitor Silva and Ricardo Ferrão

Poster Session #5

Session Chair: Ricardo Chaves (Instituto Superior Técnico /INESC-ID, Portugal)

Yet Another Many-Objective Clustering (YAMO-PACK) for FPGA CAD
Meng Yang, Jinmei Lai and Jiarong Tong

An Automatic FPGA Design and Implementation Framework
Qian Zhao, Motoki Amagasaki, Masahiro Iida, Morihiro Kuga and Toshinori Sueyoshi

A Hardware Complete Detection Mechanism for an Energy Efficient Reconfigurable Accelerator CMA
Akihito Tsusaka, Mai Izawa, Roe Uno, Nobuyuki Ozaki and Hideharu Amano

Towards a Many-Core Architecture for HPC
Janet Wyngaard, John Collins, Brian Farrimond and Michael Inggs

Aging Monitoring with Local Sensors in FPGA-Based Designs
Carlos Leong, Jorge Semião, Isabel Teixeira, Marcelino Santos, M. Valdés, Judit Freijedo, J. Rodriguez, F. Vargas, João Teixeira

Runtime Assertions and Exceptions for Streaming Systems
Tim Todman and Wayne Luk

SMI: Slack Measurement Insertion for Online Timing Monitoring in FPGAs
Joshua M. Levine, Edward Stott, George A. Constantinides and Peter Y.K. Cheung

A Framework for Hardware Cellular Genetic Algorithms: an Application to Spectrum Allocation in Cognitive Radio
Pedro Vieira dos Santos, José Carlos Alves and João Canas Ferreira

SDR Control Interface: An FPGA Based Infrastructure for Control of VPX Software Defined Radio Systems
Stefanie Castillo, Armando Astarloa, Jesus Lazaro, Sergio Salas and Isaac Ballesteros

Design and FPGA Implementation of a 100 Gbit/s Optical Transport Network Processor
Rodrigo Bernardo, Arley Henrique Salvador, Eduardo Mobilon, Luis Renato Monte, Stephane Boisclair, Avrum Warshawsky

A High Performance Deblocking Filter Hardware for High Efficiency Video Coding
Erdem Ozcan, Yusuf Adibelli and Ilker Hamzaoglu

Image Recognition Operation on a Dynamically Reconfigurable Vision Architecture
Yuki Kamikubo, Minoru Watanabe and Shoji Kawahito

Analysis of Matrix Multiplication on High Density Virtex-7 FPGA
Wilson Maltez, Ana Rita Silva, Horácio Neto and Mário Véstias

FPGA Implementation and DPA Resistance Analysis of a Lightweight HMAC Construction Based on Photon Hash Family
Susana Eiroa and Iluminada Baturone

FEMIP: A High Performance FPGA-Based Features Extractor & Matcher for Space Applications
Stefano Di Carlo, Giulio Gambardella, Piergiorgio Lanza, Paolo Prinetto, Daniele Rolfo and Pascal Trotta

Demo Presentations (Demo Night Session)

Chair: José G. F. Coutinho (Imperial College London, UK)

Hybrid FPGA-Accelerated SQL Query Processing
Louis Woods, Zsolt István and Gustavo Alonso

Rapid Modular Assembly of Xilinx FPGA Designs
Andrew Love and Peter Athanas

Remote FPGA Design Through eDiViDe - European Digital Virtual Design Lab
Jochen Vandorpe, Jo Vliegen, Ruben Smeets, Nele Mentens, Milos Drutarovsky, Michal Varchola, Kerstin Lemke-Rust, Peter Samarin, Paul Plöger, Dirk Koch, Yngve Hafting and Jim Tørresen

High Performance FPGA Object Detector
Pavel Zemčík, Roman Juránek, Petr Musil, Martin Musil and Michal Hradiš

MAMPSx: A Demonstration of Rapid, Predictable HMPSoC Synthesis
Shakith Fernando, Mark Wijtvliet, Firew Siyoum, Yifan He, Sander Stuijk, Akash Kumar and Henk Corporaal

NetThreads-10G: Software Packet Processing on NetFPGA-10G in a Virtualized Networking Environment
Stuart Byma, J. Gregory Steffan and Paul Chow

Parallel and Scalable Custom Computing for Real-Time Fluid Simulation on a Cluster Node with Four Tightly-Coupled FPGAs
Kentaro Sano, Ryo Ito, Hayato Suzuki and Yoshiaki Kono

From Quartus to VPR: Converting HDL to BLIF with the Titan Flow
Kevin E. Murray, Scott Whitty, Suya Liu and Vaughn Betz

The HercuLeS High-Level Synthesis Environment
Nikolaos Kavvadias and Kostas Masselos

Demonstration of a Heterogeneous Multi-Core Processor with 3-D Inductive Coupling Links
Yusuke Koizumi, Noriyuki Miura, Yasuhiro Take, Hiroki Matsutani, Tadahiro Kuroda, Hideharu Amano, Ryuichi Sakamoto, Mitaro Namiki, Kimiyoshi Usami, Masaaki Kondo and Hiroshi Nakamura

A Spiking Neural Network on a Portable FPGA Tablet
Matthew Naylor, Paul J Fox, A Theodore Markettos and Simon W Moore

A 64-bit MIPS Processor Running FreeBSD on a Portable FPGA Tablet
Jonathan Woodruff, A. Theodore Markettos and Simon W Moore

A Self-Adaptive Image Processing Application Based on Evolvable and Scalable Hardware
Ángel Gallego, Javier Mora, Andrés Otero, Blanca López, Eduardo de la Torre and Teresa Riesgo

SimXMD: Simulation-Based HW/SW Co-Debugging
Ruediger Willenberg and Paul Chow

IOPT-Tools - A Web based Tool Framework for Embedded Systems Controller Development Using Petri Nets
Luis Gomes, Filipe Moutinho, and Fernando Pereira

Building Partial Systems with GOAHEAD
Christian Beckhoff, Alexander Wold, Anders Fritzell, Dirk Koch and Jim Tørresen

Online Boosted Tracking Using RIFFA 2.0
Matthew Jacobsen and Ryan Kastner

Winners of the Innovate Europe Contest 2012-2013:

Co-organized by ALTERA and CNFM (National Coordination in Micro and Nanoelectronics Training, France)

Guitar Pedal
Guillermo S. Leon, ETSI Telecomunicacion, Universidad Politecnica de Valencia, Spain

Real Time Fractal Flame Rendering
Dimitrios Skarlatos, G. Mantakos, T. Stratikopoulos, Department of Electronic and Computer Engineering Technical University of Crete, Greece

ONOFF: OpenCL based non binary LDPC decoding for FPGA
João Andrade, Vitor Silva, Gabriel Falcão, Instituto de Telecomunicacões, Department of Electrical and Computer Engineering, University of Coimbra, Portugal

Exhibition (Sept. 2-4):

9:30 - 18:00	**Xilinx, Inc., Microsemi, Corp., Solflare Communications, Inc., Altera, Corp., Sigasi, nv, Dini-Group, Inc.** Exhibition Chair: Manuel Gericota (Instituto Politécnico do Porto/ISEP, Portugal)

Workshops/Tutorials (Sept. 1 and Sept. 5-6):

Sept. 1 (full-day) - Conference Hotel	**Workshop on Research Projects Focusing on High Performance Computing (HPCW'13)** **http://fpl2013-hpcw.chimait.com/** Organizers: Diana Göhringer (Ruhr-Universität Bochum, Germany), Gabriel Marchesan Almeida (Leica Biosystems, Germany), and Jürgen Becker (Karlsruhe Institute of Technology, Germany) Location: Ipanema Park Hotel, room Porto
Sept. 1 (full-day) - Conference Hotel	**Altera Workshop on Harnessing the Power of FPGAs using Altera's OpenCL Compiler** **http://www.fpl2013.org/workshops.htm#altera** Organizer: Altera Corp. Location: Ipanema Park Hotel, room Ipanema
Sept. 5-6 (two full-days) – FEUP	**Xilinx Workshop on Advanced Embedded System Design Using Zynq** **http://www.fpl2013.org/workshops.htm#xilinx** Organizer: Xilinx Inc. Location: Univ. do Porto, Faculdade de Engenharia (FEUP), room I221

Sept. 5 (full-day) – FEUP	**2nd Workshop on Self-Awareness in Reconfigurable Computing Systems (SRCS'13)** **http://srcs13.doc.ic.ac.uk** Organizers: Tobias Becker (Imperial College London, UK), Marco Platzner (University of Paderborn, Germany), and Markus Happe (ETH Zürich, Switzerland) Location: Univ. do Porto, Faculdade de Engenharia (FEUP), Room B008
Sept. 5 (half-day, morn.) - FEUP	**Embedded Reconfigurable Architectures (ERA) Tutorial** **http://www.fpl2013.org/workshops.htm#era** Organizers: Stephan Wong (Delft University of Technology, The Netherlands), and Luigi Carro (Universidade Federal do Rio Grande do Sul - UFRGS, Brazil) Location: Univ. do Porto, Faculdade de Engenharia (FEUP), Room B009
Sept. 6 (full-day) – FEUP	**Challenges of Embedded Robotics (CER'13): Can FPGAs Overcome Them?** **http://www.fpl2013.org/cer** Organizers: Vanderlei Bonato (Universidade de São Paulo/ICMC, Brazil), José Carlos Alves (Universidade do Porto/FEUP/INESC-TEC, Portugal), and Eduardo Marques (Universidade de São Paulo/ICMC, Brazil) Location: Univ. do Porto, Faculdade de Engenharia (FEUP), Room B009

Keynotes

Programmable Logic in a Software Person's World

Gordon Brebner, Distinguished Engineer, Xilinx Labs, Ireland

Monday, Sept. 2, 09:00 – 10:00, Room Ipanema

Abstract:

Programmable logic has been in the peripheral vision of computer science for the past 25 years or so. While the idea of soft hardware has seemed full of potential, productive application has been held back by two main factors: the small size of the physical devices, and the programming experience being akin to hardware chip design. The former issue has now been ameliorated by the emergence of modern FPGA devices containing millions of programmable logic gates, plus other embedded processing and memory. The latter issue is the subject of this talk. One line of attack is attempting to map general-purpose programming languages, with automatic extraction of parallelism. An alternative is to adopt a more domain-specific approach, looking to map natural domain parallelism fairly directly onto the fine-grain concurrency of the FPGA. The talk will focus on the important domain of network packet processing as an example. It has been shown that FPGAs have the raw capability to perform packet processing at very high data rates, currently around 100-200 Gb/s, with 400 Gb/s and 1.6 Tb/s on the horizon. The challenge is to allow the networking programmer in the street to describe packet processing problem instances, and automatically obtain FPGA solutions that deliver the required performance with acceptable power consumption. Some recent positive research results will be presented in the talk, and some conclusions will be drawn concerning the productive cohabitation and harnessing of programmable logic alongside other programmable processors.

Short Bio:

Dr Gordon Brebner is a Distinguished Engineer at Xilinx, Inc., the worldwide leader in programmable logic platforms. He works in Xilinx Labs, leading an international group researching issues surrounding networked processing systems of the future. His main personal research interests concern dynamically reconfigurable architectures, domain-specific languages with highly concurrent implementations, and high performance networking and telecommunications, with also a historical interest in computational complexity. He has authored numerous papers and the book Computers in Communication, and holds many patents. Prior to joining Xilinx in 2002, Gordon was the Professor of Computer Systems at the University of Edinburgh in the United Kingdom, directing the Institute for Computing Systems Architecture.

Architecting SOC FPGA's

Sean Atsatt, Altera Corp., USA

Tuesday, Sept. 3, 09:00 – 10:00, Room Ipanema

Abstract:

Silicon Convergence is the idea integrating more of the system into a single die or package. The inevitability of this integration has been proven time and again as device capacities continue to grow. With the integration of high performance processing and processor subsystems with FPGA logic come unique architecture challenges as well as opportunities. The needs of both FPGA hardware designers and software engineers must both be met not only without compromise, but with architecture and methodology to allow the two to work smoothly together. Factored into this mix is the need to meet an extremely broad set of use models across many market segments inside of a power and cost needs. This talk describes the many factors that come into play when architecting SOC FPGA's and how they affect device efficiency and usability.

Short Bio:

Sean Atsatt's 30 year career has spanned the design of Spacecraft, ASIC's for Disk Drives, Digital Cameras and Processors, and for the last 10 years FPGA. He has filled the roles of Lead Engineer, Manager and Director. Sean is probably one of the few people you will meet who has likely had their skin cells sent to Venus and Jupiter from handling flight electronics. During Sean's first 6 years at Altera he was responsible for the Nios II product line including the processor hardware, software, tools and OS ports. For the last 4 years Sean has been a member of the Altera CTO office and the lead architect for Altera's first generation of SOC FPGA's.

Accelerating The Datacenter

Satnam Singh, Google, USA

Wednesday, Sept. 4, 08:50 – 09:50, Room Ipanema

Abstract:

Reconfigurable computing ought to have significant benefits if applied in datacenters of companies like Google and Amazon. In particular, the FPGA computing community would argue about the benefits of placing highly compute intensive kernel operations onto FPGAs to reduce latency (a key metric in the performance of cloud based solutions). This is typically achieved by parallelizing an algorithm by mapping it onto the 2D or 3D spatial computing surface of an FPGA. Another benefit ought to be a reduction in the energy consumption of algorithms mapped onto FPGAs due to the careful movement of data onto and off an FPGA and the careful staging of data through customized processing elements. Energy consumption is one of the main limiting factors for deploying and scaling up datacenters. Yet FPGAs have not seen any significant deployment in datacenters as client accessible computing engines which can be used to accelerate operations like search and video processing.

This presentation will identify some of the challenges that have prevented the use of FPGAs for computing in the public cloud. In particular, the presentation will highlight the operational elements of managing a datacenter which in turn make it difficult to absorb heterogeneous computing elements. Some of these challenges can be overcome (e.g. Amazon offer GPU-based computing in its EC2 platform) and it should be possible to find similar accommodations for FPGAs. Another source of challenges arises from the mismatch between the programming models developed for using FPGAs in an embedded context (which is the current state of affairs) versus what is required to support an eco-system where FPGAs are used to accelerate the compute intensive portions of applications. The presentation will describe this mismatch in detail and highlight ways in which we can develop programming models that better suit spatial computing in the cloud. Specifically, an argument will be made for supporting "run once circuits" which are designed to be deployed and run just once and then discarded. This results in a radically different economic model for determining how to perform operations like high level synthesis and place and route.

Short Bio:

Satnam Singh is a software engineer at Google working on the configuration management of services that run on Google's datacenters. He also holds the Chair of Reconfigurable Computing at the University of Birmingham, UK. Previous he has worked at Microsoft (in the Developer Division for Visual Studio and then in

Microsoft Research), Xilinx Labs, as an academic at the University of Glasgow and also at European Silicon Structures and British Telecom.

Reconfigurable Hardware at the World's Largest Software Company

Ken Eguro, Microsoft Research in Redmond, Washington, USA

Wednesday, Sept. 4, 14:00 – 15:00, Room Ipanema

Abstract:

The large scale of cloud-based computing fundamentally changes the practical considerations for the devices one might place in a datacenter. Certain advantages can be amplified while others are reduced. Either way, this re-organizes designers' priorities and creates new opportunities.

This presentation will discuss some of the unique characteristics reconfigurable computing devices bring to the cloud, beyond their traditional role as computational accelerators, and why these capabilities are important. For example, "why is hardware virtualization so critical to the cloud?" and "can reconfigurable devices help address pervasive securities issues?"

Short Bio:

Ken joined the Embedded and Reconfigurable Computing group at Microsoft Research in Redmond, Washington in 2008. He also holds an affiliate faculty appointment in the Electrical Engineering Department at the University of Washington. Some of his past and present research interests include:

- Innovative high-performance computing architectures
- Applications of reconfigurable computing platforms
- Addressing FPGA development and integration issues
- Security concerns of hardware and security solutions using hardware
- Cryptography & cryptanalysis

Presentations and Panel: EU Horizon 2020 Reconfigurable Computing Funding Opportunities

Moderator: Cristina Silvano (Politecnico di Milano, Italy)

Wednesday, Sept. 4, 15:45 – 17:15, Room Ipanema

Invited Talks:

Horizon 2020 perspectives

Panos Tsarchopoulos, Future and Emerging Technologies, EU Project Officer

Short Bio:

Panagiotis Tsarchopoulos is a Project Officer at the ICT Research Programme of the European Commission working in the area of High Performance Computing. Dr Tsarchopoulos holds a PhD in Computer Engineering from the University of Kaiserslautern, Germany and an MBA from the UBI, Brussels, Belgium.

FPGAs in ARTEMIS – Retrospection and Prospective

Georgi Kuzmanov, ARTEMIS Joint Undertaking, Programme Officer

Short Bio:

Georgi Kuzmanov obtained his MS degree from TU Sofia in 1998 and his PhD from TU Delft in 2004. His professional experience includes a couple of years in industry as an R&D engineer and 10+ years in academia. Until 2011 he had been an assistant professor at the Computer Engineering Lab of TU Delft where he

is currently a lecturer. At TU Delft, he had been part of the Molen research team and had contributed to many research projects. In 2006, he was awarded a VENI grant from the Dutch Organization for Scientific Research (NWO) to support his research on reconfigurable scientific computer designs. In 2007, he was awarded the John Atanasoff national award of the President of the Republic of Bulgaria for his achievements in information technologies. Dr. Kuzmanov has also received the ACM ComSysTech'09 and the ACM ISC'10 best paper awards. His research interests include computer architecture, reconfigurable computing, high performance computing and cyber-physical systems. He is a co-founder of BlueBee Multicore technologies. Since November 2011 Georgi Kuzmanov has been a Programme Officer at ARTEMIS-JU, established in Brussels.

This special session will start by a first part (40 minutes expected) consisting of introductory presentations by the invited speakers, followed by a panel ***"Transitioning to Horizon2020"*** centered on discussions based on pre-defined key questions from the moderator and on open questions from the attendees.

Industry Session

The industry session consists of short presentations from industry related to products, technologies, tools, devices, and university programs. The presentations are followed by questions from the audience.

Chair: Sinan Kaptanoglu (Microsemi Corp., USA)

Tuesday, Sept. 3, 15:40 – 17:40, Room Ipanema

Exhibition

The FPL exhibition includes Xilinx, Inc., Microsemi, Corp., Solflare Communications, Inc., Altera, Corp., Sigasi, nv, and The Dini-Group, Inc.

Exhibition Chair: Manuel Gericota (Instituto Politécnico do Porto/ISEP, Portugal)

Monday-Wednesday, 09:30 – 18:00, Rooms Arrábida and Coimbra

Demo Night

At the demo night we will have 17 demonstrators from various research projects around the world showcasing their latest work in reconfigurable technology, the participation of our exhibitors and sponsors, and the participation of the winners of the Innovate Europe Contest 2012-2013. During the demo night we will have **hors d'oeuvres** and **drinks.**

Demo Night Chair: José G. F. Coutinho (Imperial College London, UK)

Monday, Sept. 2, 19:00 – 21:30, Rooms Ipanema, Arrábida and Coimbra

Birds-of-a-Feather (BoF) Sessions

Session overview and call for participation

The sessions will start with 10 minute lightning talks that will present recent work in the respective fields. The second part of the sessions will be devoted to an open discussion on the topics addressed by each BoF session and will be driven by questions submitted by the session participants.

All attendees are invited to join the BoF sessions.

BOF #1: Just-in-time compilation and runtime implementation techniques for FPGAs

Chairs: Christian Plessl (University of Paderborn, Germany), and Michael Hübner (Ruhr-Universität Bochum, Germany)

Tuesday, Sept. 3, 15:40 – 17:40, Room Porto

Overview

Despite their reconfigurability, FPGAs and other reconfigurable hardware accelerators have so far been used predominantly such that the generation of a configuration happens well before execution. Generating highly specialized, instance-specific accelerators during execution is generally possible. But the time overhead caused by the long runtimes of a state-of-the-art FPGA synthesis, placement and routing tool flow prohibits in most cases the exploitation of the additional performance that could be gained by specifically tailoring the accelerator to the application or even to the currently solved problem instance.

Over the last couple of years, foundational research efforts have been made to investigate, whether and how just-in-time compilation techniques can also be applied to reconfigurable accelerators. These efforts range from developing new tool flows that apply ideas from just-in-time compilation of software to just-in-time hardware synthesis, over improved implementation tool flows aiming at drastically reducing the time for placement and routing at runtime (e.g. by composing accelerators from predefined components) to new reconfigurable architectures that allow for very fast placement and routing. If successful, the combination of these approaches may lead to self-optimizing adaptive computing systems that

automatically move computation from the main CPU to reconfigurable accelerators allowing arbitrary applications to profit from the performance and energy-efficiency benefits of reconfigurable hardware.

This BOF session intends to bring together researchers that study aspects of just-in-time compilation for FPGAs and other reconfigurable hardware architectures in order to exchange ideas, seed a community of like-minded researchers, and to coordinate efforts on building common research platforms (tools, architectures, prototypes).

BOF #2: High-level synthesis

Chairs: Kyle Rupnow (Nanyang Technological University, Singapore), and Nikolaos Kavvadias (Ajax Compilers, Athens, Greece)

Tuesday, Sept. 3, 15:40 – 17:40, Room Granja

Overview

Current VLSI technology allows the design of sophisticated digital systems with ever-growing demands in performance and power/energy consumption. Rapidly changing user demands, unprecedented applications, evolving current or newly-introduced standards, continuously shape the computational landscape. It has long been observed that human designers' productivity does not escalate sufficiently to match the corresponding increase in chip complexity. This problem can be solved by the adoption of methodologies that raise the design abstraction level, ingeniously hiding low-level, time-consuming, error-prone details. High-level synthesis (HLS) meets all these requirements and is particularly useful in the development and orchestration of IP-based SoCs (Systems-on-a-Chip).

HLS approaches and offerings have been developed by academic groups, startups, established FPGA and EDA vendors, however there is still need to tackle important shortcomings, inefficiencies and omissions. Recent research efforts investigate several aspects of HLS such as the compilation of model-based, concurrent, and functional languages to hardware, multi-IC system partitioning, automatic source transformations for improving QoR, and power-aware synthesis issues on smaller process geometries.

This BoF session intends to bring together researchers that study aspects of high-level synthesis for FPGAs, ASICs, and heterogeneous platforms in order to exchange ideas, showcase existing work, and establish common ground for future efforts on developing a high-quality, open, extensible research infrastructure.

Social Program

Visit to Taylor's Port Wine Cellars and Banquet at the Taylor's Restaurant

On September 3rd we will have the FPL 2013 banquet at the Taylor's wine cellars restaurant "Barão de Fladgate" and appreciate one of the best views of the city of Porto. Before the dinner we will have the opportunity to visit the Taylor's wine cellars to learn about the history of the Port wine and to know more about the different varieties, flavors and curiosities of one of the finest wines in the world. Be prepared to ask questions!

Taylor's Port

Rua do Choupelo n° 250

4400-088 Vila Nova de Gaia, Portugal

GPS Coordinates: 41.134049° N, 8.613993° W

Ribeira Trip

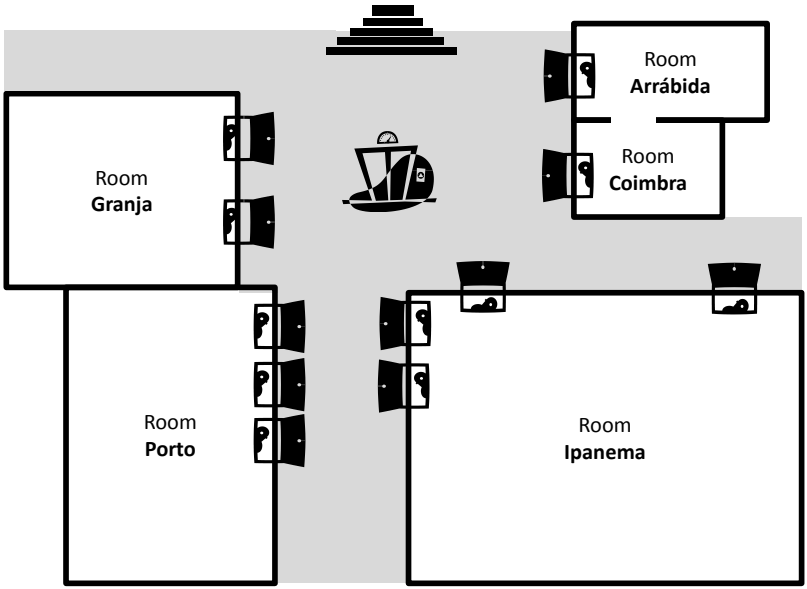
On September 4th we will have a surprise trip called "Ribeira Trip".

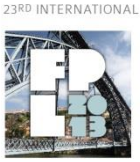
Conference Area

The main area for the conference is at the floor -1 of Ipanema Park Hotel. The rooms of the conference presentations are **Ipanema**, **Porto**, and **Granja**. The exhibition takes place at rooms **Arrábida** and **Coimbra** and the Demo night, including the hors d'oeuvres and drinks, will take place at the same floor. The poster sessions and the coffee-breaks will run at the main space between the rooms in the same floor. The Cocktail Reception (hosted by Solarflare Comm., Inc.) will run at the bar Twin Towers.

The table below summarizes the locations of the main conference activities and the map following the table shows the space of floor -1.

	Location in the Ipanema Park Hotel
Presentation rooms	Rooms **Ipanema**, **Porto**, and **Granja**
Exhibition	Rooms **Arrábida** and **Coimbra**
Demo night (including hors d'oeuvres and drinks)	All space of floor -1
Cocktail Reception (hosted by Solarflare Comm., Inc.)	Bar Twin Towers (Hotel reception floor)
Coffee-Breaks and Poster Sessions	All space between rooms of floor -1





Organization

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- **Cristina Silvano**, Politecnico di Milano, Italy
- **Michael Hübner**, Ruhr-Universität Bochum, Germany

PhD Forum Co-Chairs:

- **Miriam Leeser**, Northeastern University, USA
- **Stephan Wong**, Delft University of Technology, The Netherlands

Sponsor and Exhibition Chairs:

- **Fernando Gonçalves**, Coreworks S.A., Lisboa, Portugal
- **Manuel Gericota**, ISEP, Porto, Portugal

Demo Night Chair:

- **José G. F. Coutinho**, Imperial College London, UK

Birds of a Feather (BOF) Chairs:

- **Christian Plessl**, University of Paderborn, Germany
- **Kyle Rupnow**, Nanyang Technological University, Singapore

Track Architectures:

- **Horácio Neto**, INESC-ID/IST, Portugal
- **Ray Cheung**, City University of Hong Kong, China

Track Applications:

- **Teresa Riesgo**, Universidade Politécnica de Madrid (UPM), Spain
- **Ryan Kastner**, University of California, USA

Track Design Methods and Tools:

- **André DeHon**, University of Pennsylvania, USA
- **Guy Gogniat**, Université de Bretagne-Sud - UEB, France
- **Luigi Carro**, UFRGS, Brazil

Track Surveys, Trends and Education:

- **André DeHon**, University of Pennsylvania, USA
- **Marco D. Santambrogio**, Politecnico di Milano, Italy

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- **Pedro Silva**, Departamento de Engª Informática FEUP/ Universidade do Porto, Portugal

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Practical Information

Wi-Fi Access (free)

Coverage	All hotel area
Access information	Network Name: HFIpanemaPark Security key: hfippark Type of Key: WPA

Pre-Proceedings

USB memory stick inside the conference bag

Service Numbers

Emergency Service Numbers

SOS - Número Nacional de Socorro - 112

Police/Emergency call

Polícia Segurança Pública: (+351) 222 006 821

Guarda Nacional República: (+351) 223 399 600

Fire service/rescue control center

Batalhão Sapadores Bombeiros (B.S.B.): (+351) 225 073 700

Bombeiros Voluntários do Porto: (+351) 222 038 387

Bombeiros Voluntários Portuenses: (+351) 226 151 800

Ambulance emergency service

Cruz Vermelha Portuguesa: (+351) 226 006 353

Conference Office

Department of Informatics Engineering, Faculty of Engineering, University of Porto, Secretariat: (+351) 22 508 2134

Taxi Companies

RADITÁXIS: (+351) 225073900, (+351) 969661666/7, (+351) 917555085/6, (+351) 935073900/1

Táxis Invicta, Central Rádio Táxi do Porto: (+351) 225 076 400, (+351) 912 301 252, (+351) 934 772 174, (+351) 968 520 064

Public Transportation

Porto Metro Network

The Metro of Porto is split in zones. ANDANTE (a blue fare card) is the only title (fare card) that enables you to travel in metro network. This card can be purchased at ANDANTE stores, STCP and CP Porto sale spots, and at vending machine in any of the metro stops or stations and is rechargeable. Prior to getting on a metro or bus, you need to validate your fare by tapping the card onto one of the magnetic sensors (yellow boxes) located on the boarding platforms. It can be also used in the STCP lines, in the bus operators and in the urban trains of CP Porto.

Porto Bus Services (STCP)

Porto and its surrounds are served by an extensive bus service (called STCP).

Buses from the Hotel

The HF Ipanema Park hotel is served by three buses (no. 200, 207, and 504). The "Lordelo" bus stop, located within 50 m, is the nearest bus stop to the hotel.

From downtown Porto to the Ipanema Park hotel:

By metro:

Leaving from the "Avenida dos Aliados", continue up the street towards the "Trindade" metro station (behind the City Hall/"Câmara Municipal do Porto") and take the line A, B, C, or E, towards "Casa da Música". Exit at the "Casa da Música" metro station and take the bus no. 504 or the bus ZL ("Zona Lordelo") towards "Norteshopping". Exit the bus at the "Lordelo" bus stop (the HF Ipanema Park hotel is located within 50m).

By bus:

Leaving from the "Avenida dos Aliados", take the bus no. 200 (towards "Castelo do Queijo") or the bus no. 207 (towards "Foz-Mercado") at the "Praça D. João I" (next to the "Teatro Rivoli"). Exit the bus at the "Lordelo" bus stop (the HF Ipanema Park hotel is located within 50m).

How to get to FEUP (for the Sept. 5-6 workshops)

We suggest you take the metro to get to FEUP. FEUP is served by the D line of Metro (yellow line) and is located in the C6 zone. The D line connects the University Pole, where FEUP is located, to the Town Hall of Gaia in 15 minutes, passing through the "Trindade" metro station, where it has connection with lines A (blue), B (red), C (green) and E (violet). To get to FEUP you must get off the metro at the "IPO" metro station (see the image below), go around the "Campus S. João" Shopping Center, and take the long street ("Rua do Doutor Plácido da Costa") to its end. Then, you must cross the "Rua do Doutor Roberto Frias" road and you are at FEUP!

Universidade do Porto
Faculdade de Engenharia (FEUP)
Rua Dr. Roberto Frias, s/n
4200-465 Porto
Portugal

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